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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,514	01/30/2006	Gregory Goodhue	PHUS030253	6165

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EXAMINER	
FONG, VINCENT	
ART UNIT	PAPER NUMBER
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,514	GOODHUE ET AL.	
	Examiner	Art Unit	
	Vincent Fong	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01-30-2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application and amendment filed on 01-30-2006.

Claims 1-17 are pending and have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 01-30-2006 is being considered by the examiner.

Specification

3. The abstract of the disclosure is objected to because element number should be deleted (104, 103a,b,c,d, 200a,b,c,d). Correction is required. See MPEP § 608.01(b).

4. Claims 1,6,10,12,17 are objected to because of the following informalities: The mean of the use of term "other than" is not clear. For examination it is assume the limitation means "not". Appropriate correction is required.

5. Claims 1-17 are objected to because of the following informalities: All elements reference (e.g. 101) should be deleted from the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear that what the limitation "other than clock circuit gated" means. It is assume that the limitation means "not a clock gate circuit".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1,2,7-13 and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Broxterman et al. (USPN 6058467, hereinafter Broxterman).

As per claim 1, Broxterman discloses:

A microcontroller architecture comprising: a processor (element 24, figure 1) for processing of instruction data comprising memory access instructions (Column 4, lines 19-29) for accessing of a memory circuit (element 402, figure 4); at least a pointer memory circuit (element 402, figure 4), the memory circuit stores both pointer and

regular data(figure 3), for storing of a pointer address forming part of the instruction data; at least a pointer register (element 404, figure4) for storing a duplicate of the pointer address(column 5 lines 32-36); and, a control circuit (element rden, wren) for determining whether one of a read operation from the at least a pointer memory circuit and a write operation to the at least a pointer memory circuit is to take place, there are signals generated for read/write operation on the memory circuit, the control circuit that generate such signals is inherent exists, wherein for a write operation the control circuit stores the pointer address in the at least a pointer memory circuit and automatically stores a duplicate in the at least a pointer register (column 5 lines 44-51)and where for a read operation the control circuit utilizes the at least a pointer register to access data pointed to by a target pointer address derived from the pointer address stored therein and other than accesses the at least a pointer memory (column 6 lines 4-26).

As per claim 2, rejection of claim 1 is incorporated and Broxterman further discloses: A microcontroller architecture according to claim 1, comprising a pointer multiplexer block (element 418, figure 4) having at least an input port coupled to the at least a pointer register for receiving a pointer address and an output port for providing the pointer target address used for indirect addressing operations of data stored within the memory circuit.

As per claim 7, rejection of claim 1 is incorporarted and Broxterman further discloses:

A microcontroller according to claim 1, comprising a clock circuit (crystal) having a clock cycle (column 2 lines 21-29) and coupled to the at least a memory circuit (element 402 figure 4), the at least a pointer register(element 404 figure 4), and the control block (element 414 figure 4), wherein the read operation accesses a region in the memory circuit that is addressed by the target pointer address within a single clock cycle (column 5 lines 16-18).

As per claim 8, Broxterman discloses:
A method of pointer based addressing comprising the steps of: providing at least a pointer memory (element 402 figure 4); providing at least a pointer register (element 404 figure 4); storing of a pointer address data in the at least a pointer memory; and, upon storing of a pointer address data in the at least a pointer memory, automatically storing a duplicate pointer address data, which is a duplicate of the pointer address data, in the at least a pointer register (column 5 lines 46-52, 60-62).

As per claim 9, rejection of claim 8 is incorporated and Broxterman further discloses:
A method according to claim 8, wherein the step of automatically storing is performed within a same clock cycle as the step of storing (column 5 lines 46-52).

As per claim 10, rejection of claim 8 is incorporated and Broxterman further discloses:
A method according to claim 8, wherein the step of automatically storing is performed after the step of storing (column 5 lines 46-52), writing to memory trigger the write in the

shadow copy, such that the at least a pointer memory is not accessible by other operations until the step of automatically storing is completed; both acts of storing would complete at the same cycle which no other operation would be issued to access the memory.

As per claim 11, rejection of claim 8 is incorporated and Broxterman further discloses: A method according to claim 8 comprising the step of detecting all changes to the at least a pointer memory for automatically storing the duplicate pointer address data (column 5 lines 41-44, 46-52).

As per claim 12, rejection of claim 8 is incorporated and Broxterman further discloses: A method according to claim 8, comprising the steps of: receiving a memory access request to a memory location within a memory for retrieving of data stored at the memory location addressed by the pointer address(column 5 lines 4-5); retrieving of the duplicate pointer address data from the pointer register (column 6 lines 7-10); and, accessing the memory using a target pointer address derived from the duplicate pointer address data and not using a target pointer address derived from the pointer address data stored in the at least a pointer memory (column 6 lines16-20).

As per claim 13, rejection of claim 12 is incorporated and Broxterman further discloses:

A method according to claim 12, comprising the step of providing a clock circuit having a clock cycle, wherein the steps of receiving , retrieving and accessing are performed in a single clock cycle (column 5 lines 16-18).

As per claim 15, rejection of claim 12 is incorporated and Broxterman further discloses: A method according to claim 12, comprising the step of detecting all changes to the at least a pointer memory for automatically storing the duplicate pointer address data (column 5 lines 41-44, 46-52).

As per claim 16, rejection of claim 12 is incorporated and Broxterman further discloses: A method according to claim 12, wherein the at least a pointer register comprises a plurality of pointer registers (element 404 figure 4), wherein the step of accessing comprises the step of multiplexing of the pointer address data (element 418 figure 4) stored in the plurality of pointer registers to form the target pointer address for accessing of the random access memory (column 6 lines16-20).

As per claim 17, Broxterman discloses:
A storage medium having data (hardware design language) stored thereon (column 6 28-32), the data for implementation of a processing system comprising: first instruction data for providing at least a pointer memory (element 402 figure 4); second instruction data for providing at least a pointer register (element 404 figure 4); third instruction data for upon storing of a pointer address in the at least a pointer memory, automatically

storing a duplicate pointer address, which is a duplicate of the pointer address, in the at least a pointer register (column 5 lines 41-44, 46-52); fourth instruction data for receiving a memory access request (indirect instruction)to a memory location within a memory for retrieving of data stored at the memory location addressed by the pointer address(column 4 lines 19-29); fifth instruction data for retrieving of the duplicate pointer address from the at least a pointer register(column 6 lines 15-20); and, sixth instruction data for accessing the memory using a target pointer address derived from the duplicate pointer address and other than using a target pointer address derived from the pointer address stored in the at least a pointer memory(column 6 lines 15-20).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broxterman in view of Agrawal et al. (USPN 5179716, hereinafter Agrawal).

As per claim 3, rejection of claim 2 is incorporated and Broxterman discloses the limitations of claim 2.

Broxterman does not discloses a source select block that has three inputs.

However Agrawal discloses a microcontroller architecture comprising a source select block (element 304 figure 11) having a first input port for receiving a next program

address derived from a current program counter value plus a length of a current instruction(element 316 figure 11), a second input port for receiving the pointer target address from the pointer multiplexer block (element 292 figure 11), a third input port for receiving a selection signal (element 312 figure 11, column 16 lines 32-34)from the control circuit for determining which data bits from the at least one of the input signals received at the first and second input ports are to be used for providing of pointer data output signals from output ports of the source select block.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Broxterman inventions to incorporate Agrawal inventions. One of ordinary skill in the art would be motivated to make such modification to provide flexible I/O to the system (column 3 lines 58-60).

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broxterman in view of Agrawal as applied to claim 3 above, and further in view of Born et al. (USPN 6131108, hereinafter Born).

As per claim 4, rejection of claim 3 is incorporated and the combination of Broxterman and Agrawal discloses the limitations of claim 3.

Neither Broxterman nor Agrawal discloses an input multiplexer that couple with the output of the source select block.

However Born discloses a microcontroller architecture wherein the at least a pointer register comprises a plurality of pointer registers (element 12 figure 1 column 3 lines 18-20, each 16 bit segment represent a pointer), the microcontroller architecture

comprising an input multiplexer (element 16 figure1)having input ports coupled to the pointer data output signals therefrom (signals from element 12 figure 1), and for receiving of an input data multiplexer control signal from the control block (element 22 figure 1), the input multiplexer control signal for determining which data bits derived from the pointer data output signals are to be used in forming of the pointer address for storage in the plurality of pointer registers (column 3 lines 24-28).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Broxterman and Agrawal to incorporate Born inventions. One of ordinary skill in the art would be motivated to make such modification to simplify the circuit design for generate multi bit output (column 2 lines 21-24).

13. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Broxterman in view of Agrawal further in view of Born as applied to claim 4 above, and further in view of Nukiyama (USPN 4926312).

As per claim 5, rejection of claim 4 is incorporated and the combination of Broxterman, Agrawal and Born discloses the limitation of claim 4.

Neither one of Broxterman, Agrawal and Born discloses the output multiplexer.

However, Nukiyama discloses a microcontroller architecture wherein the at least a pointer memory circuit comprises a plurality of pointer memory circuits (element 20,28 figure 1), the microcontroller architecture comprising an output multiplexer (element 24 figure 1) having input ports coupled to plurality of pointer memory circuits for receiving of data bits derived from the stored pointer address stored within the plurality of pointer

memory circuits and having an output port for providing a program counter value (address register)for being restored during a return (RET) from interrupt instruction (column 4 lines 30-37).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Broxterman Agrawal and Born to incorporate Nukiyama inventions. One of ordinary skill in the art would be motivated to make such modification to make the system able to perform skip operation without having substantial performance hit (column 3 lines 45-47).

As per claim 6, rejection of claim 5 is incorporated the combination of Broxterman, Agrawal, Born and Nukiyama discloses the limitation of claim 5.

Broxterman further discloses a pointer multiplexer (element 418 figure 4) that is not a clock gate circuit; no clock input to the pointer multiplexer.

Neither one of Broxterman, Agrawal and Nukiyama discloses an input multiplexer.

However, Born discloses an input multiplexer (element 304 figure 11) that is not a clock gate circuit; no clock input to the input multiplexer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Broxterman, Agrawal and Nukiyama to incorporate Born inventions. One of ordinary skill in the art would be motivated to make such modification to simplify the circuit design for generate multi bit output (column 2 lines 21-24).

Neither one of Broxterman, Agrawal and Born discloses an output multiplexer.

However, Nukiyama discloses an output multiplexer (element 304 figure 11) that is not a clock gate circuit; no clock input to the output multiplexer.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Broxterman, Agrawal and Born to incorporate Nukiyama inventions. One of ordinary skill in the art would be motivated to make such modification to make the system able to perform skip operation without having substantial performance hit (column 3 lines 45-47).

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broxterman in view of Born.

As per claim 14, rejection of claim 12 is incorporated and Broxterman discloses the limitation of claim 12.

Broxterman doesnot disclose the write back of target pointer address.

However Born discloses a method comprising the step of writing back the target pointer address (element 36 figure 1) to the pointer storage (element 12 figure 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Broxterman inventions to incorporate Born inventions. One of ordinary skill in the art would be motivated to make such modification to simplify the circuit design for generate multi bit output (column 2 lines 21-24).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Amdahl discloses an extra pointer storage to save clock cycle in execute indirect address instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on Monday to Thursday from 7:00 to 4:30. The examiner can also be reached on alternate Friday from 7:00 to 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Fong VF
January 5, 2007

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1/8/07